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| 10/586,810 | 07/21/2006 | Philippe Meunier-Beillard | US04 0056 US2 | 8780 |

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| EXAMINER | |
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| DOYLE, JOHN | |
| **ART UNIT** | **PAPER NUMBER** |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/586,810 | MEUNIER-BEILLARD ET AL. | |
| | Examiner | Art Unit | |
| | JOHN DOYLE | 2891 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on 7/21/2006.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 7/21/2006.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 5, 8-9, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Imai (US Patent 5,506,427).

In re claim 1, Imai discloses a method for growing a mono-crystalline emitter for a bipolar transistor, comprising: providing a trench (Fig. 1A, (25)) formed on a silicon substrate (10) having opposed silicon oxide side walls (Fig. 2, (34)); selectively growing a highly doped mono-crystalline layer (38; Column 4, lines 12-14) on the silicon substrate in the trench; and non-selectively growing a second silicon layer (40) over the trench in order to form an amorphous or polysilicon layer (Column 4, lines 48-50) over the silicon oxide sidewalls.

In re claim 2, Imai discloses a method wherein the step of selectively growing a highly doped mono-crystalline layer (Fig. 1D, (38)) is accomplished using selective epitaxial growth (Column 4, lines 12-14).

In re claim 5, Imai discloses a method wherein the mono-crystalline layer (Fig. 1D, (38)) is substantially grown only on an active area (14; Column 3, lines 38-42) on the silicon substrate.

In re claim 8, Imai discloses a method for forming a highly n-type doped layer in a semiconductor wafer, comprising: providing a first active region comprised of a silicon substrate (Fig. 1H, (14)); providing a second region comprised of silicon oxide (34); selectively growing a highly doped monocrystalline layer (38; Column 4, lines 12-14) on the silicon substrate; and non-selectively growing a second silicon layer (40) over the silicon substrate and silicon oxide to form an amorphous or polysilicon layer (Column 4, lines 48-50) over the silicon oxide.

In re claim 9, Imai discloses a method wherein the step of selectively growing a highly doped mono-crystalline layer (Fig. 1H, (38)) is accomplished using selective epitaxial growth (Column 4, lines 12-14).

In re claim 12, Imai discloses a method wherein the mono-crystalline layer (Fig. 1H, (38)) is substantially grown only on the active region (14).

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imai (US Patent 5,506,427) in view of Koshimizu et al. (Pub. No. US 2005/0181569 A1)

In re claim 3, Imai discloses a method for growing a mono-crystalline emitter for a bipolar transistor, comprising: providing a trench (Fig. 1A, (25)) formed on a silicon substrate (10) having opposed silicon oxide side walls (Fig. 2, (34)); selectively growing a highly doped mono-crystalline layer (38; Column 4, lines 12-14) on the silicon substrate in the trench; and non-selectively growing a second silicon layer (40) over the trench in order to form an amorphous or polysilicon layer (Column 4, lines 48-50) over the silicon oxide sidewalls. Imai discloses all the limitations except for a method wherein the selective epitaxial growth using a precursor from the group consisting of: $SiH_2Cl_2$, $SiH_4$, $SiCl_4$, $SiCl_3$, $Si_2H_6$, $Si_3H_8$, $GeH_4$, and $SiH_3CH_3$. Whereas Koshimizu et al. disclose a method wherein a selective epitaxial growth using a precursor from the group consisting of: $SiH_2Cl_2$, $SiH_4$, $SiCl_4$, $SiCl_3$, $Si_2H_6$, $Si_3H_8$, $GeH_4$, and $SiH_3CH_3$ (¶ 56) in order to form an HBT base region and an HBT emitter region (¶ 56). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the method of Imai by using a precursor from the group consisting of: $SiH_2Cl_2$, $SiH_4$, $SiCl_4$, $SiCl_3$, $Si_2H_6$, $Si_3H_8$, $GeH_4$, and $SiH_3CH_3$ in order to form an HBT emitter region, as taught by Koshimizu et al.

In re claim 10, Imai discloses a method for forming a highly n-type doped layer in a semiconductor wafer, comprising: providing a first active region comprised of a silicon substrate (Fig. 1H, (14)); providing a second region comprised of silicon oxide (34); selectively growing a highly doped monocrystalline layer (38; Column 4, lines 12-14) on the silicon substrate; and non-selectively growing a second silicon layer (40) over the silicon substrate and silicon oxide to form an amorphous or polysilicon layer (Column 4,

lines 48-50) over the silicon oxide. Imai discloses all the limitations except for a method wherein the selective epitaxial growth using a precursor from the group consisting of: $SiH_2Cl_2$, $SiH_4$, $SiCl_4$, $SiCl_3$, $Si_2H_6$, $Si_3H_8$, $GeH_4$, and $SiH_3CH_3$. Whereas Koshimizu et al. disclose a method wherein a selective epitaxial growth using a precursor from the group consisting of: $SiH_2Cl_2$, $SiH_4$, $SiCl_4$, $SiCl_3$, $Si_2H_6$, $Si_3H_8$, $GeH_4$, and $SiH_3CH_3$ (¶ 56) in order to form an HBT base region and an HBT emitter region (¶ 56). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the method of Imai by using a precursor from the group consisting of: $SiH_2Cl_2$, $SiH_4$, $SiCl_4$, $SiCl_3$, $Si_2H_6$, $Si_3H_8$, $GeH_4$, and $SiH_3CH_3$ in order to form an HBT emitter region, as taught by Koshimizu et al.

Claims 4, 11, 15, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imai (US Patent 5,506,427) in view of Schiz et al. (Leakage Current Mechanisms in SiGe HBTs Fabricated Using Selective and Nonselective Epitaxy, IEEE Transactions on Electron Devices, Vol. 48, No. 11, November 2001)

In re claim 4, Imai discloses a method for growing a mono-crystalline emitter for a bipolar transistor, comprising: providing a trench (Fig. 1A, (25)) formed on a silicon substrate (10) having opposed silicon oxide side walls (Fig. 2, (34)); selectively growing a highly doped mono-crystalline layer (38; Column 4, lines 12-14) on the silicon substrate in the trench; and non-selectively growing a second silicon layer (40) over the trench in order to form an amorphous or polysilicon layer (Column 4, lines 48-50) over the silicon oxide sidewalls. Imai discloses all the limitations except for a method wherein

the step of non-selectively growing the second silicon layer is accomplished using differential epitaxial growth. Whereas Schiz et al. disclose a method which uses differential epitaxy to grow polysilicon (Introduction) in order to fabricate a heterojunction bipolar transistor (Abstract). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the method of Imai by growing the second silicon layer with differential epitaxy growth in order to fabricate a heterojunction bipolar transistor, as taught by Schiz et al.

In re claim 11, Imai discloses a method for forming a highly n-type doped layer in a semiconductor wafer, comprising: providing a first active region comprised of a silicon substrate (Fig. 1H, (14)); providing a second region comprised of silicon oxide (34); selectively growing a highly doped monocrystalline layer (38; Column 4, lines 12-14) on the silicon substrate; and non-selectively growing a second silicon layer (40) over the silicon substrate and silicon oxide to form an amorphous or polysilicon layer (Column 4, lines 48-50) over the silicon oxide. Imai discloses all the limitations except for a method wherein the step of non-selectively growing the second silicon layer is accomplished using differential epitaxial growth. Whereas Schiz et al. disclose a method which uses differential epitaxy to grow polysilicon (Introduction) in order to fabricate a heterojunction bipolar transistor (Abstract). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the method of Imai by growing the second silicon layer with differential epitaxy growth in order to fabricate a heterojunction bipolar transistor, as taught by Schiz et al.

In re claim 15, Imai discloses a method for growing a mono-crystalline emitter for a bipolar transistor, comprising: providing a trench (Fig. 1B, (25)) formed on a substrate (10) having opposed silicon oxide side walls (Fig. 1E, (34)); growing a highly doped layer (Fig. 1G, (36, 38)) on the substrate in the trench using selective epitaxial growth (Column 4, lines 12-14); and growing a second layer (Fig. 1H, (40)) over the trench in order to form an amorphous or polysilicon layer (Column 4, lines 48-50) over the silicon oxide sidewalls. Imai discloses all the limitations except for using differential epitaxial growth to form the second layer. Whereas Schiz et al. disclose a method wherein differential epitaxy growth is used to form a polysilicon layer (Introduction) in order to fabricate a heterojunction bipolar transistor (Abstract). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the method of Imai by forming the second layer with differential epitaxy growth in order to fabricate a heterojunction bipolar transistor, as taught by Schiz et al.

In re claim 17, Imai discloses a method wherein the highly doped layer comprises a mono-crystalline layer (Fig. 1D, (38)) that is substantially grown only on an active area (14; Column 3, lines 38-42) on the silicon substrate.

Claims 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imai (US Patent 5,506,427) in view of Verma et al. (Pub. No. US 2005/0079678 A1)

In re claim 6, Imai discloses a method for growing a mono-crystalline emitter for a bipolar transistor, comprising: providing a trench (Fig. 1A, (25)) formed on a silicon

substrate (10) having opposed silicon oxide side walls (Fig. 2, (34)); selectively growing a highly doped mono-crystalline layer (38; Column 4, lines 12-14) on the silicon substrate in the trench; and non-selectively growing a second silicon layer (40) over the trench in order to form an amorphous or polysilicon layer (Column 4, lines 48-50) over the silicon oxide sidewalls. Imai discloses all the limitations except for performing a salicidation process using a silicide selected from the group consisting of: titanium, cobalt, and nickel. Whereas Verma et al. disclose a method comprising performing a salicidation process using a silicide (Fig. 9, (904, 905, 906)) selected from the group consisting of: titanium, cobalt, and nickel (¶ 70) in order to fabricate a heterojunction bipolar transistor (Abstract). Therefore it would have been obvious to one skilled in the art to modify the method of Imai by performing a salicidation process using a silicide selected from the group consisting of: titanium, cobalt, and nickel in order to fabricate a heterojunction bipolar transistor, as taught by Verma et al.

In re claim 13, Imai discloses a method for forming a highly n-type doped layer in a semiconductor wafer, comprising: providing a first active region comprised of a silicon substrate (Fig. 1H, (14)); providing a second region comprised of silicon oxide (34); selectively growing a highly doped monocrystalline layer (38) on the silicon substrate; and non-selectively growing a second silicon layer (40) over the silicon substrate and silicon oxide to form an amorphous or polysilicon layer (Column 4, lines 48-50) over the silicon oxide. Imai discloses all the limitations except for performing a salicidation process using a silicide selected from the group consisting of: titanium, cobalt, and nickel. Whereas Verma et al. disclose a method comprising performing a salicidation

process using a silicide (Fig. 9, (904, 905, 906)) selected from the group consisting of: titanium, cobalt, and nickel (¶ 70) in order to fabricate a heterojunction bipolar transistor (Abstract). Therefore it would have been obvious to one skilled in the art to modify the method of Imai by performing a salicidation process using a silicide selected from the group consisting of: titanium, cobalt, and nickel in order to fabricate a heterojunction bipolar transistor, as taught by Verma et al.

Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imai (US Patent 5,506,427) in view of Frei et al. (US Patent 6,509,242 B2)

In re claim 7, Imai discloses a method for growing a mono-crystalline emitter for a bipolar transistor, comprising: providing a trench (Fig. 1A, (25)) formed on a silicon substrate (10) having opposed silicon oxide side walls (Fig. 2, (34)); selectively growing a highly doped mono-crystalline layer (38; Column 4, lines 12-14) on the silicon substrate in the trench; and non-selectively growing a second silicon layer (40) over the trench in order to form an amorphous or polysilicon layer (Column 4, lines 48-50) over the silicon oxide sidewalls. Imai discloses all the limitations except for a method wherein the mono-crystalline emitter is n-typed doped with an element selected from the group consisting of: phosphorous and arsenic. Whereas Frei et al. disclose a method wherein the mono-crystalline emitter is n-typed doped with an element selected from the group consisting of: phosphorous and arsenic (Column 3, lines 49-53) in order to fabricate a heterojunction bipolar emitter (Abstract). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the method of Imai by n-type

doping the mono-crystalline emitter with an element selected from the group consisting of: phosphorous or arsenic in order to fabricate a heterojunction bipolar emitter, as taught by Frei et al.

In re claim 14, Imai discloses a method for forming a highly n-type doped layer in a semiconductor wafer, comprising: providing a first active region comprised of a silicon substrate (Fig. 1H, (14)); providing a second region comprised of silicon oxide (34); selectively growing a highly doped monocrystalline layer (38) on the silicon substrate; and non-selectively growing a second silicon layer (40) over the silicon substrate and silicon oxide to form an amorphous or polysilicon layer (Column 4, lines 48-50) over the silicon oxide. Imai discloses all the limitations except for a method wherein the highly n-typed doped layer is doped with an element selected from the group consisting of: phosphorous and arsenic. Whereas Frei et al. disclose a method wherein the highly n-typed doped layer is doped with an element selected from the group consisting of: phosphorous and arsenic (Column 3, lines 49-53) in order to fabricate a heterojunction bipolar emitter (Abstract). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the method of Imai by doping the highly n-doped layer with an element selected from the group consisting of: phosphorous or arsenic in order to fabricate a heterojunction bipolar emitter, as taught by Frei et al.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Imai (US Patent 5,506,427) and Schiz et al. (Leakage Current Mechanisms in SiGe HBTs Fabricated Using Selective and Nonselective Epitaxy, IEEE Transactions on Electron

Devices, Vol. 48, No. 11, November 2001) as applied to claim 15 above, and further in view of Koshimizu et al. (Pub. No. US 2005/0181569 A1)

In re claim 16, Imai and Schiz et al. disclose a method for growing a mono-crystalline emitter for a bipolar transistor, comprising growing a highly doped layer on the substrate in a trench using selective epitaxial growth. Imai and Schiz et al. disclose all the limitations except for a method wherein the selective epitaxial growth using a precursor from the group consisting of: $SiH_2Cl_2$, $SiH_4$, $SiCl_4$, $SiCl_3$, $Si_2H_6$, $Si_3H_8$, $GeH_4$, and $SiH_3CH_3$. Whereas Koshimizu et al. disclose a method wherein a selective epitaxial growth using a precursor from the group consisting of: $SiH_2Cl_2$, $SiH_4$, $SiCl_4$, $SiCl_3$, $Si_2H_6$, $Si_3H_8$, $GeH_4$, and $SiH_3CH_3$ (¶ 56) in order to form an HBT base region and an HBT emitter region (¶ 56). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the method of Imai by using a precursor from the group consisting of: $SiH_2Cl_2$, $SiH_4$, $SiCl_4$, $SiCl_3$, $Si_2H_6$, $Si_3H_8$, $GeH_4$, and $SiH_3CH_3$ in order to form an HBT emitter region, as taught by Koshimizu et al.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Imai (US Patent 5,506,427) and Schiz et al. (Leakage Current Mechanisms in SiGe HBTs Fabricated Using Selective and Nonselective Epitaxy, IEEE Transactions on Electron Devices, Vol. 48, No. 11, November 2001) as applied to claim 15 above, and further in view of Verma et al. (Pub. No. US 2005/0079678 A1)

In re claim 18, Imai and Schiz et al. disclose a method for growing a mono-crystalline emitter for a bipolar transistor. Imai and Schiz et al. disclose all the limitations

except for a step of performing a salicidation process using a silicide from the group consisting of: titanium, cobalt, and nickel. Whereas Verma et al. disclose a method comprising performing a salicidation process using a silicide (Fig. 9, (904, 905, 906)) selected from the group consisting of: titanium, cobalt, and nickel (¶ 70) in order to fabricate a heterojunction bipolar transistor (Abstract). Therefore it would have been obvious to one skilled in the art to modify the method of Imai by performing a salicidation process using a silicide selected from the group consisting of: titanium, cobalt, and nickel in order to fabricate a heterojunction bipolar transistor, as taught by Verma et al.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Imai (US Patent 5,506,427) and Schiz et al. (Leakage Current Mechanisms in SiGe HBTs Fabricated Using Selective and Nonselective Epitaxy, IEEE Transactions on Electron Devices, Vol. 48, No. 11, November 2001) as applied to claim 15 above, and further in view of Frei et al. (US Patent 6,509,242 B2)

In re claim 19, Imai and Schiz et al. disclose a method for growing a mono-crystalline emitter for a bipolar transistor. Imai and Schiz et al. disclose all of the limitations except for a method wherein the mono-crystalline emitter is n-typed doped with an element selected from the group consisting of: phosphorous and arsenic. Whereas Frei et al. disclose a method wherein the mono-crystalline emitter is n-typed doped with an element selected from the group consisting of: phosphorous and arsenic (Column 3, lines 49-53) in order to fabricate a heterojunction bipolar emitter (Abstract).

Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the method of Imai by n-type doping the mono-crystalline emitter with an element selected from the group consisting of: phosphorous or arsenic, as taught by Frei et al.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Imai (US Patent 5,506,427) and Schiz et al. (Leakage Current Mechanisms in SiGe HBTs Fabricated Using Selective and Nonselective Epitaxy, IEEE Transactions on Electron Devices, Vol. 48, No. 11, November 2001) as applied to claim 15 above, and further in view of Asai et al. (US Patent 6,455,364 B1)

In re claim 20, Imai and Schiz et al. disclose a method for growing a mono-crystalline emitter for a bipolar transistor. Imai and Schiz et al. disclose all the limitations except for a method wherein the mono-crystalline emitter is p-typed doped using boron. Whereas Asai et al. disclose a method wherein the mono-crystalline emitter (Fig. 1, (111)) is p-typed doped using boron Column 12, lines 3-21) in order fabricate a hetero bipolar transistor and a SiGe-BiCMOS device (Column 7, lines 24-28). Therefore it would have been obvious to one skilled in the art at the time of the invention to modify the method of Imai and Schiz et al. by p-typed doping the mono-crystalline emitter with boron in order to fabricate a hetero bipolar transistor and a SiGe BiCMOS device, as taught by Asai et al.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN DOYLE whose telephone number is (571)270-7879. The examiner can normally be reached on Monday-Thursday 7:30 AM-6:00PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kiesha Rose can be reached on (571)272-1844. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JOHN DOYLE
Examiner
Art Unit 2891

/JOHN DOYLE/
Examiner, Art Unit 2891

/Kiesha L. Rose/

Supervisory Patent Examiner, Art Unit 2891